AMENDMENT TO THE SPECIFICATION

Please replace the second paragraph on page 12 of the specification with the following amended paragraph:

Figure 2c is representative of further fabrication processes in accordance with the invention. In these fabrication processes, a SiGe layer 45a is grown in the channels 45 of the nFET to a height of about 100 Å to 300 Å, although other heights are also contemplated by the invention. In one embodiment, the Ge content of the SiGe may be from 0% to 50% in ratio to the Si content, preferably about 15%. Then, an epitaxial Si layer 60 is selectively grown over the SiGe layer 45a in the nFET channels 45. A sacrificial gate oxide layer 65 is then grown over the selectively grown Si layer 60. An nFET mask and well implant is then provided using any well known fabrication process. A gate oxide ~~65a~~ 65b is then formed in the nFET regions. A gate polysilicon ~~70a~~ 70b in then deposited followed by chemical mechanical polishing, well known to those of ordinary skill in the art, to produce the structure shown in Figure 2c.